**module ADD16 (A, B, S, C);**

**input [15:0] A, B;**

**output [15:0] S;**

**output C;**

**assign {C, S} = A+B;**

**endmodule**

**module Mazzay;**

**// Inputs**

**reg [15:0] inputA, inputB;**

**// Outputs**

**wire [15:0] Sum;**

**wire Carr;**

**// Instantiate the Unit Under Test (UUT)**

**ADD16 dut (inputA, inputB, Sum, Carr);**

**initial begin**

**// Initialize Inputs**

**inputA = 16'hFFFF;**

**inputB = 16'hFFFF;**

**#10**

**inputA = 16'hABCD;**

**inputB = 16'h0000;**

**#10**

**inputA = 16'h9111;**

**inputB = 16'h8765;**

**end**

**endmodule**